Qihang (Charlie) Wu

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RESEARCH INTERESTS

Electronic Design Automation (EDA), Computer Architecture, Heterogeneous Integration (HI) IC Design

EDUCATION

Arizona State University, *Ira A. Fulton Schools of Engineering*, Tempe, Arizona, United States
- Ph.D. in Computer Engineering — Started Jan 2026

New York University, *Tandon School of Engineering*, Brooklyn, New York, United States
- M.S. in Electrical Engineering — Aug 2022 – May 2024

University of Portland, *Shiley School of Engineering*, Portland, Oregon, United States
- B.S. in Computer Science — Aug 2015 – May 2020
- B.S. in Mechanical Engineering — Aug 2015 – May 2020

Sophia University, Tokyo, Japan
- Exchange Student — Jun 2017 – Aug 2017

PUBLICATION

- **Qihang Wu** and Austin Rovinski. 2025. Revisiting Hardware Priority Queue Architectures. Workshop Abstract. 2025 Open-Source Computer Architecture Research (OSCAR 2025) Workshop, Tokyo, Japan.
- **Qihang Wu**, Aman Arora and Vidya A. Chhabria. 2026. CHICO-Agent: An LLM Agent for the Cross-layer Optimization of 2.5 D and 3D Chiplet-based Systems. In Proceedings of the IEEE International Conference on LLM-Aided Design 2026.
- Zesong Jiang, **Qihang Wu**, Bing-Yue Wu and Jeff Zhang. 2026. CAPO: Certification-Guided Agentic Workflow for Physical Design Parameter Optimization. In Proceedings of the Great Lakes Symposium on VLSI 2026.
- **Qihang Wu**, Taizun Jafri, Aman Arora and Vidya A Chhabria. 2026. VPR-Evolve: Multi-Agent-Driven Algorithm Evolution for FPGA Place and Route. In Proceedings of the 32th Asia and South Pacific Design Automation Conference.

PRESENTATION

- CHICO-Agent: An LLM Agent for the Cross-layer Optimization of 2.5 D and 3D Chiplet-based Systems. Presented at the IEEE International Conference on LLM-Aided Design 2026, Stanford University, Stanford, CA, United States. Jul 2026
- Revisiting Hardware Priority Queue Architectures. Presented at 2025 Open-Source Computer Architecture Research Workshop, Waseda University, Tokyo, Japan. Jun 2025
- NASA Lunabotics 2020 (University of Portland - Robotics). Poster presented at 2019 Oregon NASA Space Grant Consortium, Oregon State University, Corvallis, OR, United States. Nov 2019

ADDITIONAL RESEARCH EXPERIENCE

High-Efficiency SRAM Design for IoT Devices
- Student Research Assistant Intern (supervised by Dr. Azeez Bhavnagarwala) — Sep 2023 – Mar 2024
  - Designed a 4kB SRAM array using **ASAP7** 7nm PDK in Cadence Virtuoso, focusing on low-power and high-density integration for IoT applications
  - Optimized **wordline and bitline decoder sizing**, improving **read/write access latency** and **power efficiency** under process variations
  - Conducted **Monte Carlo** simulations, ensuring robustness to **process-voltage-temperature (PVT)** variations
  - Performed **parasitic extraction** and **post-layout simulations**, verifying functional stability and leakage reduction techniques

SRAM Design Against Side-Channel Attacks
- Student Research Assistant Intern (supervised by Dr. Azeez Bhavnagarwala) — Oct 2022 – Mar 2023
  - Designed and synthesized an **AES-128** encryption/decryption hardware accelerator using **ASAP7 7nm PDK** in **Cadence Genus**, targeting **side-channel attack resistance**
  - Developed a **gate-level netlist** and transistor-level **HSPICE power model**, enabling **power consumption analysis** for cryptographic security evaluation
  - Simulated **Differential Power Analysis (DPA)** attacks on the AES block using **HSPICE transient simulations**, extracting power traces to assess cryptographic vulnerabilities
  - Identified correlation between power fluctuations and AES internal operations, developing insights for countermeasure development in **secure SRAM design**

ACADEMIC PROJECTS

RISC-V RV32I Multi-Cycle Processor Implementation — Fall 2023
- Designed and implemented a 32-bit NYU-6463-RV32I processor using **Verilog**, supporting a subset of the **RISC-V** RV32I Instruction set, with a focus on **microarchitecture optimization** for **FPGA deployment**

- Conducted performance and area analysis, identifying **critical paths** and ensuring **synthesizability** and **optimal resource utilization** on FPGA
- Developed a comprehensive test suite, including **unit-tests** (ALU operations, branching, memory access) and **integration tests** (RC5 encryption/decryption, control flow validation), verifying correct execution at the instruction and system levels
- Implemented **hardware interfacing modules**, enabling interaction with **external peripherals** such as switches and LEDs, demonstrating real-world I/O operations
- **Synthesized** and deployed the design on a **Basys 3 Artix-7** FPGA Trainer Board, ensuring successful **timing closure** and **functional verification**

SRAM with BIST Engine Spring 2023

- Designed and implemented a 256×4-bit SRAM using **SystemVerilog** in Cadence Virtuoso
- Verified SRAM functional correctness by integrating **SPICE**-level simulations with Behavioral RTL models
- Developed and embedded a **Built-In Self-Test (BIST) engine**, implementing industry-standard test patterns
- Synthesized the SRAM-BIST system using Cadence GENUS, **optimizing for area, power and timing constraints**
- Performed **static timing analysis (STA)** in Synopsys PrimeTime ensuring timing closure

INDUSTRIAL EXPERIENCE

Artly AI, Seattle, Washington, USA

- Hardware System Engineer Jun 2020 – May 2022
- *Artly AI (formerly known as Artly Coffee) is a Seattle-based robotic start-up developing an AI-powered robotic barista with the goal of automating and enhancing the coffee preparation process. Raised over **350 Million dollars** on StartEngine.*
  - Created innovative and customized **hardware designs** for components that improve the system's stability and expand the robot's functionality.
    - Integrated high-precision scales (0.1g accuracy, 0.01g resolution) into the robotic system, **enhancing measurement accuracy by 80%**, improving beverage consistency.
    - Designed and built a motorized rotating and tilting platform; **achieved a 120% increase in latte art success rate**.
  - Developed **embedded firmware (C, Arduino, ESP8266, STM32)** for various components used for the robotic system interfacing with the robotic control system, improving hardware-software integration.

ACHIEVEMENTS

PATENT

- "SYSTEM AND METHOD FOR ROBOTIC FOOD AND BEVERAGE PREPARATION USING COMPUTER VISION", PCT/US21/33430 May 2021

CERTIFICATION

- Oregon State Board of Examiners for Engineering, Engineer in Training (E.I.T.) Jun 2020

AWARD

- Undergraduate Team Experience Award – OGSC 2019 – 2020

ACADEMY

- Spring 2018 Dean's List May 2018